REMARKS

Please reconsider the application in view of the foregoing amendments and the following remarks.

Status of Claims

Claims 1-3 are pending in the present application. Applicants herein amend claim 1 with the subject matter of claim 2 and further defining the language of claim 1 by adding the language "generated by an oscillation circuit ..." in claim 1. Claim 2 is herein cancelled. Claim 3 is herein amended to correct the dependency thereof. New claim 4 has been added. No new matter has been entered.

Specification

Applicants herein amend the title of the application in conformance with the Examiner's suggestion in the Office Action dated December 30, 2008. Applicants appreciate the Examiner's consideration of this matter.

As to the Merits

As to the merits of this case, the Examiner sets forth the following rejections:

The Examiner has rejected claim 1 under 35 U.S.C. 102(b) as being anticipated by **Remson** (US 5,070,439).

The Examiner has rejected claims 2 and 3 under 35 U.S.C. § 103(a) as being unpatentable over **Remson** in combination with **Kates** (US 5,430,641).

Each of these rejections is respectfully traversed.

Independent claim 1

Claim 1, as amended, is drawn to ... *a switching-means driving circuit which maintains said switching means at an ON state until the AC output voltage from said AC power generator exceeds a predetermined value generated by an oscillation circuit when compared in a comparator circuit and starts the duty control with said switching means at the time when said AC output voltage exceeds the predetermined value, wherein the switching-means driving circuit includes said oscillation circuit and said comparator circuit.*

For example, as noted in paragraphs [0019] and [0020] of the present specification, "[...] The drive circuit 13 outputs driving signals for bringing **the FET 11 into conduction/non-conduction (turning on/turning off the FET 11).** There is provided a PWM circuit 14 for generating PWM signals (pulse signals) which determine the duty (on-time ratio) of the driving signals output from the drive circuit 13. **The PWM circuit 14 includes an oscillation circuit (see the detail thereof in Fig. 3) 23 for generating a reference voltage (triangular wave) Vref**

which determines the duty of the PWM signals. There is provided a **comparator 15** which makes **a comparison between the reference voltage Vref and the voltage resulted from the voltage division with the resistances 9 and 10.** If the voltage resulted from the voltage division with the resistances 9 and 10 is smaller than the reference voltage Vref, the PWM circuit 14 outputs PWM signals with a duty of 100 %, in order **to maintain the FET 11 at an ON state.** On the other hand, if the voltage resulted from the voltage division with the resistances 9 and 10 is greater than the reference voltage Vref, the PWM circuit 14 outputs PWM signals with a duty less than 100 % which is determined on the basis of the reference voltage Vref and the voltage resulted from the voltage division with the resistances 9 and 10."

In other words, the FET 11 (switching means) is maintained in an ON state if the reference voltage Vref generated by the Oscillation circuit is greater than Vout (Fig. 2) by having the switching-means driving circuit (13, 14) providing a signal with a duty cycle of 100%. However, when the Vout becomes greater than Vref, the switching-means driving circuit (13, 14) starts the duty control by outputting signal with a duty cycle less than 100% based on the comparison between the Vref and Vout.

On page 3, item 5, it is acknowledged that Remsen does not disclose the above-noted feature of amended claim 1. Nonetheless, it is alleged that "Kates discloses that a power supply device (figure 2) performing duty cycle control (pulse width modulation) on a non-insulation type DC/DC converter (Ql, Dl, C1, and L1) that starts when the input voltage exceeds a

predetermined value and starting operation of a self-excited oscillation type converter (Q2, Q3, TI, D2, D3, and C4) before the input voltage reaches the predetermined value was old and known in the art at the time of the invention."

It is respectfully submitted that the Examiner is mischaracterizing the reference. Specifically, Kates discloses the following in column 3 and column 4, the relevant portion of which are set forth below see columns 3 and 4 of Kates reference:

> "[t]he prior art inverter of FIG. 2 operates as follows. Vin connects to a low voltage DC source, such as a battery at 7 volts, and pass FET Q1 together with free-wheeling Schottky diode D1, inductor L1, **plus capacitor C1 form a buck regulator to step Vin down to Vreg = Vin X the duty cycle of pass FET Q1 [switching means]**. Pulse width modulator PWM samples the current through cold cathode fluorescent lamp CCFL-1 by tapping resistor R3 and uses this feedback to drive the gate of pass FET Q1 to control its duty cycle and thus the voltage delivered ... Resistors R5, R3, and R4, diodes D2 and D3, and capacitor C4 provide a sampling of the CCFL current for feedback to pulse width modulator PWM ... **If the voltage in the secondary circuit is too high, then pulse width modulator PWM will lower the duty cycle of pass FET Q 1 and thereby lower Vreg which implies smaller collector currents and thus smaller secondary voltage.**"

In other words, in Kates, a low voltage DC voltage (Vin) from an outside source such as battery is connected to switching means (FET Q1) a barrier diode (D1), inductor L1 and capacitor C1 in order to regulate Vin down to Vreg (reference voltage). It is to be noted that, in Kates, the Vreg is function of a low voltage Vin and the duty cycle of switching means (FET Q1) which means that if the voltage in the secondary winding (T1-S, Fig. 2) is too high, then pulse width modulator PWM (driving circuit) will lower the duty cycle of pass FET Q 1 (switching means and in turn the Vreg will also be lowered. That is, unlike the claimed invention, the driving circuit in Kates is not required to maintain switching means (FET Q1) at ON state. In fact, if the voltage in the secondary circuit is too high, then pulse width modulator PWM will lower the duty cycle of pass FET Q 1 and thereby lower Vreg which implies smaller collector currents and thus smaller secondary voltage as noted above.

In contrast, for example, in the claimed invention, the FET 11 is maintained in an ON state if the reference voltage Vref generated by the Oscillation circuit is greater than Vout by having the switching-means driving circuit providing a signal with a duty of 100%. However, when the Vout becomes greater than Vref, the switching-means driving circuit starts the duty control by outputting signal with a duty less than 100% based on the comparison between the Vref and Vout.

Therefore, it is respectfully submitted that Remson and Kates, alone or in combination, do not disclose *a switching-means driving circuit which maintains said switching means at an ON state until the AC output voltage from said AC power generator exceeds a predetermined value generated by an oscillation circuit when compared in a comparator circuit and starts the duty control with said switching means at the time when said AC output voltage exceeds the predetermined value, wherein the switching-means driving circuit includes said oscillation circuit and said comparator circuit.* Therefore, it is requested that the rejection under 35 U.S.C. §102 and §103 be withdrawn.

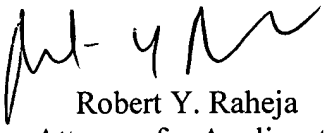
Conclusion

The Claims have been shown to be allowable over the prior art. Applicants believe that this paper is responsive to each and every ground of rejection cited in the Office Action dated December 30, 2008, and respectfully request favorable action in this application. The Examiner is invited to telephone the undersigned, applicants' attorney of record, to facilitate advancement of the present application.

If this paper is not timely filed, Applicants respectfully petition for an appropriate extension of time. The fees for such an extension or any other fees that may be due with respect to this paper may be charged to Deposit Account No. 50-2866.

Respectfully submitted,

WESTERMAN, HATTORI, DANIELS & ADRIAN, LLP



Robert Y. Raheja
Attorney for Applicants
Registration No. 59,274
Telephone: (202) 822-1100
Facsimile: (202) 822-1111

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